AIP Journal of Applied Physics

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Citation: Journal of Applied Physics **115**, 014106 (2014); doi: 10.1063/1.4861033
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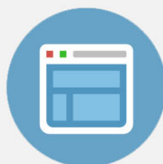

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Degradation characteristics of metal/Al_2O_3/n-InGaAs capacitors

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(Received 17 September 2013; accepted 15 December 2013; published online 6 January 2014)

Implementation of new materials in Metal-Oxide-Semiconductor stacks requires capabilities to predict long-time degradation as well as the impact of process changes on degradation processes. In this work, the degradation under constant voltage stress of metal gate/Al_2O_3/InGaAs stacks is studied for different pre-dielectric deposition treatments. The results show that the degradation, particularly under negative bias, is strongly affected by the oxide-semiconductor surface treatment of the samples. Two contributions (interface states and bulk traps) dominate depending on the stress conditions. Surface treatment with NH_4OH shows a better quality of the interface in term of interface states; however, it contributes to generation of positive charge on the dielectric layer. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4861033]

I. INTRODUCTION

InGaAs is an attractive candidate to be used as a channel material for the extension of CMOS (Complementary Metal-Oxide-Semiconductor) technology beyond Si due to its high electron mobility.[1] Lacking a good native oxide interface, a major challenge is the reduction of the density of interface states, since it causes Fermi level pinning, leading to degradation of charge concentration in the channel and thus affecting the response of metal-oxide-semiconductor field effect transistors (MOSFETs).[2]

Recent works have focused on the control of surface oxidation since the creation of interface states is often attributed to semiconductor surface oxidation.[3–5] In particular, the influence of pre-dielectric deposition NH_4OH treatment on the oxide-semiconductor interface to suppress the formation of surface oxidation has been studied. Lebedev *et al*. have reported that NH_4OH significantly reduces the amount of Ga_2O_3 on GaAs surface,[6] and Krylov *et al*. have suggested that NH_4OH suppresses the formation of Ga-O bonds, which are related to interface states at the Al_2O_3/InGaAs interface.[7] The pre-deposition NH_4OH treatment suppresses efficiently the XPS peaks of sub-oxides; however, the impact of NH_4OH treatment on the degradation of the MOS stacks has not been studied in detail.

Implementation of new materials in actual devices requires capabilities to predict long-time degradation as well as the impact of process changes on degradation processes. Recently, some papers have reported on studies of the degradation of high-k dielectric/InGaAs stacks,[8–10] but much more knowledge is needed to understand the degradation mechanism and the influence of the fabrication process. Among the recent results, Wrachien *et al*.[8] have reported the effects of stress polarity on the degradation of Al_2O_3/InGaAs stacks, and Huang *et al*.[9] found out that the inclusion of an interlayer on ZrO_2/InGaAs improves the performance of nFETs. However, in both cases, the influence of the oxide-semiconductor interfaces on the mechanisms involved in the degradation has not been studied in detail. Particularly, much effort has been performed to reduce the density of border traps and/or interface states, but more information is needed to describe and model the mechanisms responsible for the degradation on high-k dielectric/InGaAs stacks.

In this work, the influence of the oxide-semiconductor interface on the degradation is studied by the dynamics of the flat band voltage (V_{FB}) under different polarities of the stress voltage. In the first part of the manuscript, the quality of the Al_2O_3/InGaAs interface treated by NH_4OH and its influence on the electrical characterization are analyzed, while the second part is focused on the study of the dynamics of degradation of the flat band voltage (V_{FB}) and the generation of defects at interfaces of the stack.

II. EXPERIMENTAL

In this work, two different sets were used on n-type InGaAs substrates epitaxially grown on InP wafers. In one set (set A), a pre-dielectric deposition treatment (PDT) was performed by a 36% NH_4OH solution. Then, a 9 nm-Al_2O_3 layer was prepared by atomic layer deposition (ALD) using trimethylaluminium (TMA) and H_2O precursors at 300 °C. In set B, a 9 nm—Al_2O_3 film was deposited by the same ALD process but without the NH_4OH PDT. In both sets, the area of the devices was $1.1 \times 10^{-4}\,cm^2$, and the gate metallization consisted of Ti(1 nm)/Au(200 nm) deposition followed by post deposition annealing (PDA) at 400 °C in N_2 flow for 30 min. Further details about the samples can be found in our previous work, Ref. 7.

Capacitance–Voltage (C-V) measurements were carried out at different frequencies using an Agilent 4285A LCR meter. Current-Voltage (I-V) and constant-voltage-stress (CVS) measurements were performed using an Agilent 4155C parameter analyzer. During CVS, the stress was periodically interrupted for C-V measurements to track the degradation of the device parameters such as V_{FB}. For each stress condition, a dozen of devices were measured.

To avoid recovery-related artifacts,[11] we kept constant values of the delay time between the C-V measurements and the CVS pulses. The calculation of V_{FB} was performed by the recently introduced inflection point technique.[12]

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III. RESULTS AND DISCUSSIONS

A. Influence of the oxide-semiconductor interface on electrical characteristics

One of the most common approaches for interfaces-state characterization in MOS stacks is to measure the capacitance–voltage characteristics over a wide range of frequencies.[7,13,14] Figure 1 shows typical multi-frequency C-V curves of the two sets. Set A, treated by NH_4OH (Fig. 1(a)), shows a relatively small increase of the capacitance in the inversion regime; while in set B, no NH_4OH treatment (Fig. 1(b)), the capacitance is increased significantly in this regime. This dispersion in inversion is defined in literature as "weak inversion hump" and is attributed to Al_2O_3/InGaAs interface states.[13,15] As reported in our previous work,[7] the origin of such differences between both sets is due to the NH_4OH treatment, which when applied suppresses the formation of Ga-O bonds in the Al_2O_3/InGaAs interface, which was clearly correlated with the decrease of interface.

The area under the C-V hump (Q_{hump}) measured at 100 kHz, which is related to the density of interface states,[15] shows a reduction from 4.67 $\times 10^{-7}$ Q/cm^2 to 2.5 $\times$ 10^{-7} Q/cm^2 for set A (treated with NH_4OH), indicating the efficiency of this treatment for Al_2O_3/InGaAs gate stacks.

On the other hand, it is observed in Fig. 1 that the dispersion with frequency of the accumulation capacitance is small and similar for both sets of samples, indicating no influence of the NH_4OH treatment on the border traps density in the vicinity of the Al_2O_3 interface.[16] Moreover, Table I shows similar C-V hysteresis results for both sets indicating also a similar density of border traps.[17–19]

TABLE I. Description of C-V hysteresis at RT.

Set	Fresh	After CVS for 15 min@ −4.8 V&27 °C	After CVS for 15 min@ −4.8 V&125 °C
	ΔV_{FB}^{Hyst} (V) ± %10	ΔV_{FB}^{Hyst} (V) ± %10	ΔV_{FB}^{Hyst} (V) ± %10
Set A	0.15	0.20	0.30
Set B	0.13	0.19	0.31

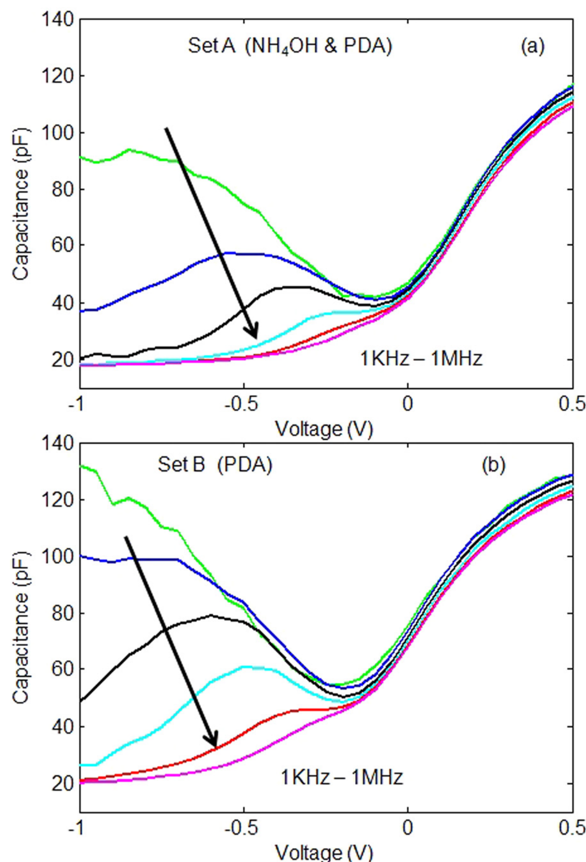

FIG. 1. Typical multi-frequency capacitance-voltage curves from 1 KHz to 1 MHz. (a) Set A. (b) Set B. Arrows mark the direction of frequency increase.

Figure 2 shows typical current-voltage (I-V) curves for both sets. For positive bias, both sets shows a similar behaviour; while for negative bias, at low voltages, set B shows initial current levels higher than those of set A (treated by NH_4OH). Note that the comparison of the I-V curves of both sets is consistent with the analysis of the C-V curves of Figure 1.

In n-type InGaAs stacks, the positive-bias-voltage region (i.e., accumulation) is dominated by interaction of border traps.[2,19,20] Therefore, the similarity in the I-V curves at positive bias can be explained by a similar density of border traps in both sets,[8] since the defects in the oxide that are likely to impact the I-V curves are those that result in charge-transition levels within the Fermi-level range.

At negative voltages, the increase of the leakage current, observed in Figure 2, resembles the stress-induced-leakage-current (SILC) of ultrathin SiO_2 layers in MOS structures,[21] since at high voltages both I-V curves show the same behaviour. As the Fermi level goes into the lower part of the band gap towards the valence band, due to negative bias applied on the gate, the energy levels of defects above the semiconductor conduction band edge are empty, thus allowing carriers to tunnel into them, increasing the leakage current through the gate dielectric.[21] Hence, a difference in the density of defects may result in difference on the I-V characteristics.

The negative-bias voltage region is dominated by interaction with interface states,[2,19,20] the density of which is higher in set B. Therefore, such as increase of the interface states can be responsible for the difference in the I-V curves. Moreover,

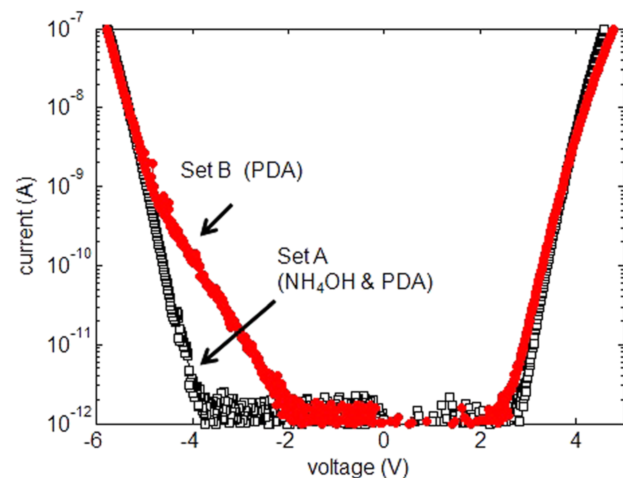

FIG. 2. Typical current-voltage characteristics for both sets.

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Krylov *et al.*[15] showed that the Ga-O bonds (present in set B as reported in our previous work Ref. 7) may create energy levels located near mid gap in InGaAs, and Weber *et al.*[22] showed that oxygen vacancies (such as Ga-O) in Al_2O_3/InGaAs stacks introduce energy levels that can contribute to the leakage current through the gate dielectric. Therefore, it is reasonable to assume that the Ga-O bonds present in set B[7] contribute defects that increase the leakage current.

B. Degradation characteristics of the C-V curves

In order to study the degradation characteristics, the devices were subjected to CVS of both polarities applied on the gate with the other terminal (wafer's back contact) grounded. In this section, the main characteristics of C-V curves after single pulses of voltage stress are analyzed for both sets. Figures 3(a) and 3(b) show typical CVS measurements with positive polarity for both sets, where the current was continuously measured as function of time, for voltages ranging from +3.5 V to +5.2 V. Note that the initial current levels are similar for both samples, indicating similarities in the current-voltage characteristics as observed in Figure 2. Regarding the degradation, it is relevant to mention that only the early stage of the CVS is going to be considered, where the SILC is negligible, since the post-breakdown characteristics of these MOS structures are out of the scope of this work. At high voltages and longer times, large current variations are observed that can be related to large amounts of damage in the dielectric layer. This evolutionary behaviour resembles the soft-breakdown event of ultrathin SiO_2 layers in MOS structures.[21]

During the early stage of the CVS, the main characteristic is a decrease of the current with a constant slope ($\alpha = -0.17$), namely an indication of a power law dependence ($log(I) \sim \alpha . log(V)$). This constant degradation rate over a large stress bias range is a clear indication that the first stage of degradation for positive stress bias is dominated by negative charge trapping independently of the voltage.[23] We believe that the decrease of the gate current can be ascribed to existing bulk/border Al_2O_3-InGaAs traps. A recent work[20] shows that the tunneling of electrons into the border traps near the oxide/semiconductor interface in Al_2O_3/InGaAs plays a significant role in accumulation. Since the density of border traps seems to be similar for both sets based on similar dispersion in frequency of the accumulation capacitance;[14,16] and on similar C-V hysteresis measurement (see Table I),[17–19] it could be assumed that the constant degradation rate was caused by similar densities of border traps in both sets of samples. The degradation was also studied by multi-frequency C-V curves. Figures 3(c) and 3(d) show a comparison of the C-V curves before (curves marked by squares) and after (continuous lines) a positive stress pulse of +5 V for 100 s. It is clear that the C-V curves shift towards positive bias (negative charge trapping) and that the weak inversion hump, which is related to the density of interface states,[14,16] does not show any significant variation; after the stress pulse, the area under the C-V hump (Q_{hump}) measured at 100 kHz[15] shows a small variation of around 10%. Note that this behavior is consistent with the results of Figures 3(a) and 3(b) where negative charge trapping dominates. A different scenario is found out for negative bias CVS. The first observation, in the I-V curves of Figure 2 discussed above, is that at low voltages, set B shows initial current levels higher than those of set A, but this difference diminishes as the voltage is increased showing similar levels from −4.8 V. Therefore, the comparison of CVS characteristics between both sets should be performed for stress voltages ranging from −4.8 V in order to obtain similar current levels during the experiment. Figures 4(a) and 4(b) show typical CVS measurements with negative polarity in this regime

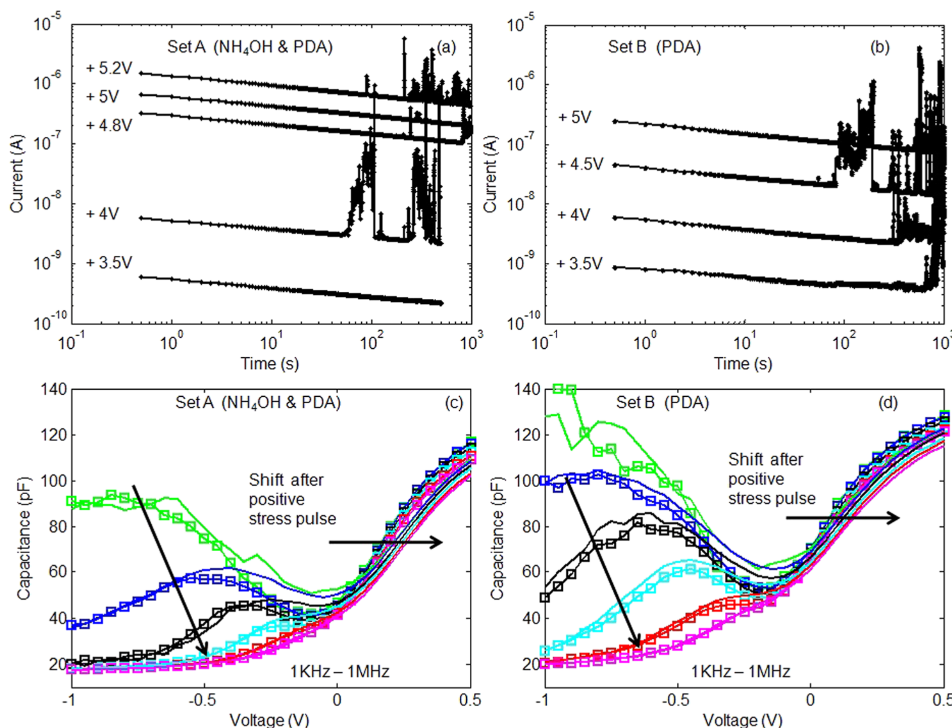

FIG. 3. Typical measurements of current as function of the time under constant voltage stress for the Set A (a), and Set B (b). Typical multi-frequency capacitance-voltage curves from 1 KHz to 1 MHz before (curves marked by squares) and after (continuous lines) a positive stress pulse for Set A (c), and Set B (d).

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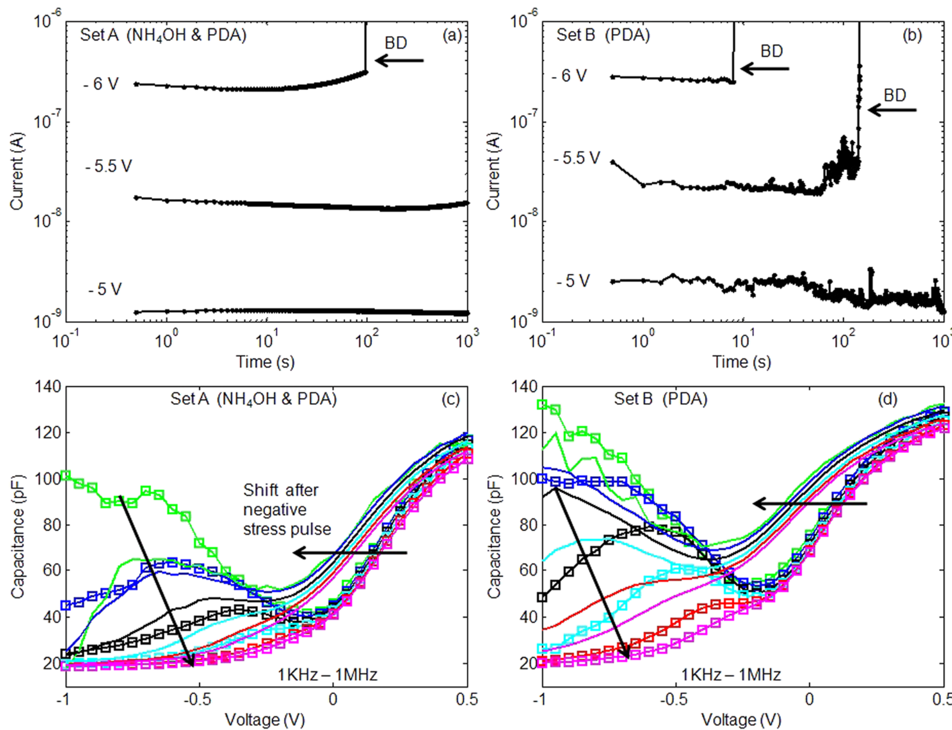

FIG. 4. Typical measurements of current as function of the time under constant voltage stress for the set A (a), and Set B (b). Typical multi-frequency capacitance-voltage curves from 1 KHz to 1 MHz before (curves marked by squares) and after (continuous lines) a negative stress pulse for Set A (c), and Set B (d). The breakdown event of the gate oxide is marked by sign BD.

for both sets, where the current was continuously measured as function of time. These figures show that the main characteristic is a significant increase in the fluctuations of the current for set B. The physical origin of the randomly fluctuated current profile observed in the early stage of the CVS experiment is originated from defects in the oxide.[24] It is believed that this phenomenon is related to the trapping/detrapping of carriers in the dielectric.[21,24] At positive bias, in the early stage of the CVS, the fluctuations of the current are not observed since the degradation is dominated by electron trapping into the borders traps near the interface.[20]

Although the study of the variations of the gate current is not the scope of this work, it is important to note that such fluctuations on the gate current are consistent with the observation in Figure 2, where the increase of the leakage current at low voltage is a clear indication of defects in the dielectric that can contribute to the fluctuation of the current.[21,24] For the set A, at low voltages, the current level is constant; while at higher voltages, it is observed an increase of the current near the breakdown event (BD) due to the stress-induce-leakage-current (SILC).[21]

Figures 4(c) and 4(d) show the effect of degradation in the multi-frequency C-V curves after a single pulse of -5 V for 100 s. We observe a shift of the C-V curves towards negative bias (positive charge trapping), and an increase of the weak inversion hump suggesting generation of interface states.[14,16] It is observed that after the stress pulse at negative bias, the area under the C-V hump (Q_{hump}) at 100 kHz (related with the interface states) for both sets shows a significant increase of 40%. The overall results obtained so far show that the degradation under constant voltage stress behaves differently under positive and negative bias stresses, in agreement with previous works.[8,9] and we find that the surface treatment with NH_4OH affect the CVS at negative bias.

C. Evolution of V_{FB} under constant voltage stresses

In order to understand the root-cause of the degradation phenomena, we studied the evolution of the degradation manifested in the C-V characteristics. For this purpose, CVS experiments were performed and the stress was periodically interrupted to measure the V_{FB} by C-V curves (at 500 KHz). Figure 5 shows the shift of V_{FB} (ΔV_{FB}) as function of the stress time at +3 V on the gate electrode (positive gate bias) at room temperature (27 °C) for both sets. It is observed that sets A and B show a similar behavior suggesting a common degradation mechanism. Moreover, it is observed in the inset of Figure 5 that V_{FB} (calculated after CVS at +3 V for 30 s) does not show temperature dependence. Note that the insensitivity of ΔV_{FB} to temperature is consistent with trapping of

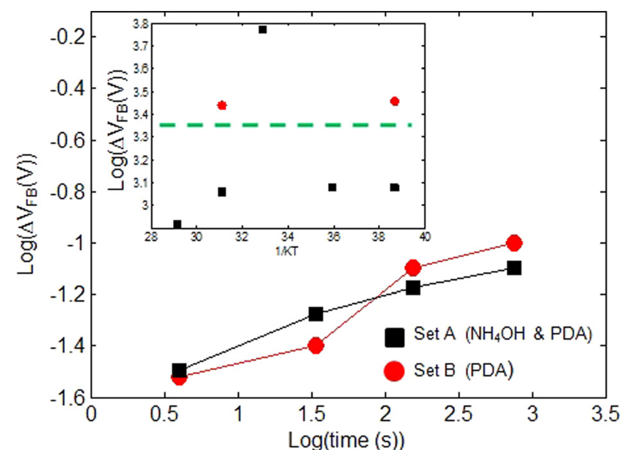

FIG. 5. Time evolution of the shift of the flat-band voltage (ΔV_{FB}) after CVS pulses at +3 V at room temperature (27 °C). The inset shows the dependence of the shift of the flat band voltage (ΔV_{FB}) as function of the temperature for both sets. In this case, V_{FB} is calculated after CVS at +3 V for 30 s for both cases.

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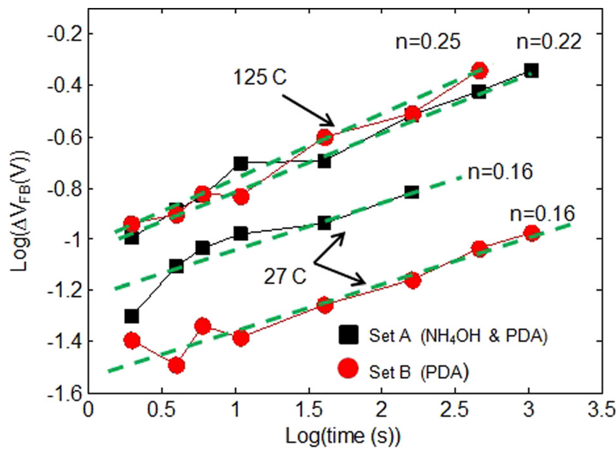

FIG. 6. Time evolution of the shift of the flat-band voltage (ΔV_{FB}) after CVS pulses at −4.8 V for both sets at 27 °C and 125 °C.

electrons tunneling from the channel into native traps in the oxide during positive bias stress.[23,25]

Figure 6 shows for both sets ΔV_{FB} as function of the stress time for a stress voltage of −4.8 V (negative gate bias) at two temperatures. At room temperature (27 °C), it is clear that set A (treated with NH_4OH) shows a larger shift at the same stress time; while at a high temperature (125 °C), both sets show similar behavior. It is important to note that the differences in the ΔV_{FB} values are not an artifact due to differences in the initial V_{FB} for both sets of samples. The comparison for the same value of V_G-V_{FB} in both sets will only increase a little the difference of ΔV_{FB} observed at RT in Figure 6; while at high temperatures, the dependence with the stress voltage is weak and the comparison for the same value of V_G-V_{FB} in both sets will not change the main observations.

Figure 7 shows ΔV_{FB} as function of 1/KT for both set of samples at negative stress polarity. It shows that the activation energy under negative bias stress is much higher than in the case of positive bias stress (inset Figure 5), and different for both sets. Set A (treated with NH_4OH) shows an

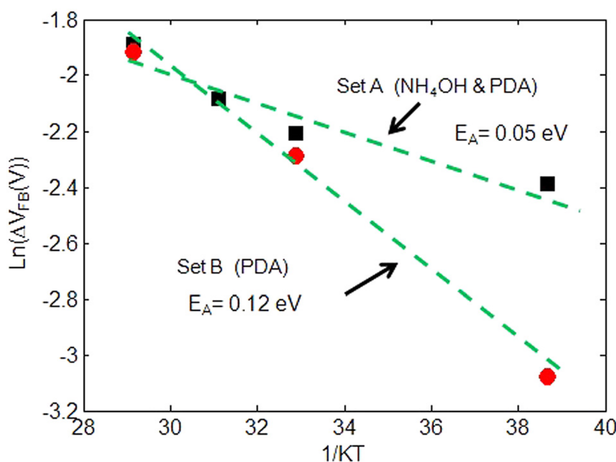

FIG. 7. Dependence of the shift of the flat band voltage (ΔV_{FB}) as function of the temperature for both sets. (a) The flat band voltage is calculated after CVS at +3 V for 30 s. (b) The flat band voltage is calculated after CVS at −4.8 V for 6 s.

activation energy ($E_A = 0.05$ eV) much lower than set B ($E_A = 0.12$ eV), indicating that the two contributions to the positive charge mentioned above hold a different temperature dependence.

The positive oxide charge generated under negative gate bias can be understood in terms of the dissociation of the bonds at the interface (i.e., depassivation of the interface). This interpretation assumes that when a negative gate voltage is applied, it initiates a field-dependent reaction at the oxide-semiconductor interface that generates positive charges breaking the passivated bonds at the interface.[8,26–29] Particularly, Wrachien *et al.*[8] suggested this mechanism to explain the different trapped charge polarity observed under CVS at positive and negative bias in Al_2O_3/InGaAs stacks. In our case, for set A, due to the pre-deposition treatment with NH_4OH followed by post deposition annealing (PDA) at 400 °C in N_2, it is expected to have an Al_2O_3/InGaAs interface more N-rich than set B. It is important to note that in standard gate oxides, it has been demonstrated that nitrogen plays a relevant role at the semiconductor-oxide interface in the generation of positive charge when negative bias is applied,[28] suggesting that similar effects could occurs in Al_2O_3/InGaAs stacks.

In our experimental conditions, set A shows a better interface quality, which is associated with the suppression of Ga-O bonds by the treatment with NH_4OH and PDA as reported in our previous work Ref. 7. Taking into account this aspect, the origin of ΔV_{FB} differences may be attributed to the different densities of passivated Ga-O bonds between the two sets. Set A consists of a much larger density of passivated bonds (an aspect that was confirmed by XPS in our previous work[7]); therefore under a de-passivation process (such as a negative stress bias), set A contributes a larger positive charge than set B, explaining the different curves at 27 °C in Figure 6.

At high temperatures, an additional mechanism seems to dominate the generation of positive charge. This is a reasonable interpretation, since both sets (with a low or a high number of passivated Ga-O bonds) show a similar behavior in Figure 6; and at high temperatures, the existing bonds (Ga-O and others) could be easily broken under stress[27,30] and contribute to the shift of V_{FB}. The experimental evidence that supports this assumption are the C-V hysteresis measurements before and after CVS pulses at −4.8 V at 125 °C and 27 °C (see Table I). The C-V hysteresis calculated at flat band is an indication of charged defects, namely border traps.[17–19] Note that the C-V hysteresis measurement was done in a retrace mode where the voltage was swept from inversion to accumulation and back to inversion. All the C-V hysteresis measurements were performed at 27 °C. The voltage shift due to the hysteresis loop was calculated at C_{FB} capacitance ($\Delta V_{FB}^{Hysteresis}$),[19] which could related with the trapped charge by $Q_{trapped} = \Delta V_{FB}^{Hyst}.\varepsilon_o.k/t_{ox}$.[19,25] Further details about the calculation of ΔV_{FB}^{Hyst} can be found in Ref. 31.

It is observed in Table I that ΔV_{FB}^{Hyst} is much larger after a CVS pulse at a high temperature (125 °C), than after a CVS pulse at RT (27 °C), which is a clear indication that the generation of border traps is much relevant at high temperatures. Since the degradation at RT is mainly dominated by the

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interface (as discussed in Figure 6), the generation of border traps during CVS at a high temperatures supports our assumption that an additional degradation mechanism is present in this condition.

Another important observation from the results of Figure 6 is the evolution with temperature of the slope (n) of the ΔV_{FB} curves. At room temperature, the ΔV_{FB} curves show a power-law time dependence with an exponent $n = 0.16$ for both sets; while at high temperatures, the exponent increases to $n = 0.22$–0.25. It is important to mention that a similar exponent on both sets is a clear indication of occurrence of a similar degradation process. These observations agree with literature where a power-law dependence with $n = 0.16$ is reported at room temperature in several publications,[26–28] and an increase of the exponent with temperature in the range of 0.20–0.30 is observed as well.[27,30,32] The increase of the time exponent at high temperatures also supports the existence of an additional degradation component. At accelerated stress conditions (high T), it is possible to generate positive bulk traps causing an additional contribution to the degradation of the oxide-semiconductor interface increasing the time exponent[26,31,33] and over-riding the room temperature mechanism.

D. Interface states

The analysis of interface states (D_{it}) generation is a relevant aspect since the main mechanism at negative bias seems to be strongly affected by the quality of the oxide-semiconductor interface.

Figures 8(a) and 8(b) show the parallel conductance $G_P/A.w.q$ contours plots for fresh devices of sets A and B, respectively; a different behavior is observed between them. The traces in the middle of the conductance plots represent the conductance peaks. Since the band bending is correlated with the shift in the frequency of the maximum of the normalized conductance peak $[G_P/A.w.q]_{max}$ as a function of gate bias,[34] the change in $[G_P/A.w.q]_{max}$ with respect to certain gate bias change reflects the trap density level at the oxide-semiconductor interface.[2,34] High D_{it} creates high drag to $[G_P/A.w.q]_{max}$ movement. Set A shows that $[G_P/A.w.q]_{max}$ moves vertically across the map, indicating that the band bending is efficient. In contrast, set B shows a marked frequency shift with gate bias, indicating much larger density of interface states.[2,34] Moreover, the magnitude of $[G_P/A.w.q]_{max}$ for set B (Fig. 8(b)) is much larger than for set A (Fig. 8(a)), also an indication of a high density of interface states. Note that this observation is consistent with the previous results of Figure 1, where set A shows a lower "weak inversion hump" due to low density of D_{it} by reduction of the Ga-O bonds as results of the PDT treatment.[7]

Figures 8(c) and 8(d) show such analysis of the $[G_P/A.w.q]$, but after degradation by CVS at −4.8 V. In set A, there is a marked frequency shift with gate bias, and an increase of the magnitude of $[G_P/A.w.q]_{max}$, both indicating a much larger density of interface states after stress at negative bias. On the other hand in set B, there is only a small increase of the frequency shift with gate bias (compared to the fresh state), and no change of the magnitude of $[G_P/A.w.q]_{max}$.

It is clear that under negative stress bias, the generation of positive charge (showed by ΔV_{FB} shift on Figure 6) is accompanied with generation of interface states. Set A with an smaller initial density of interface states (an aspect

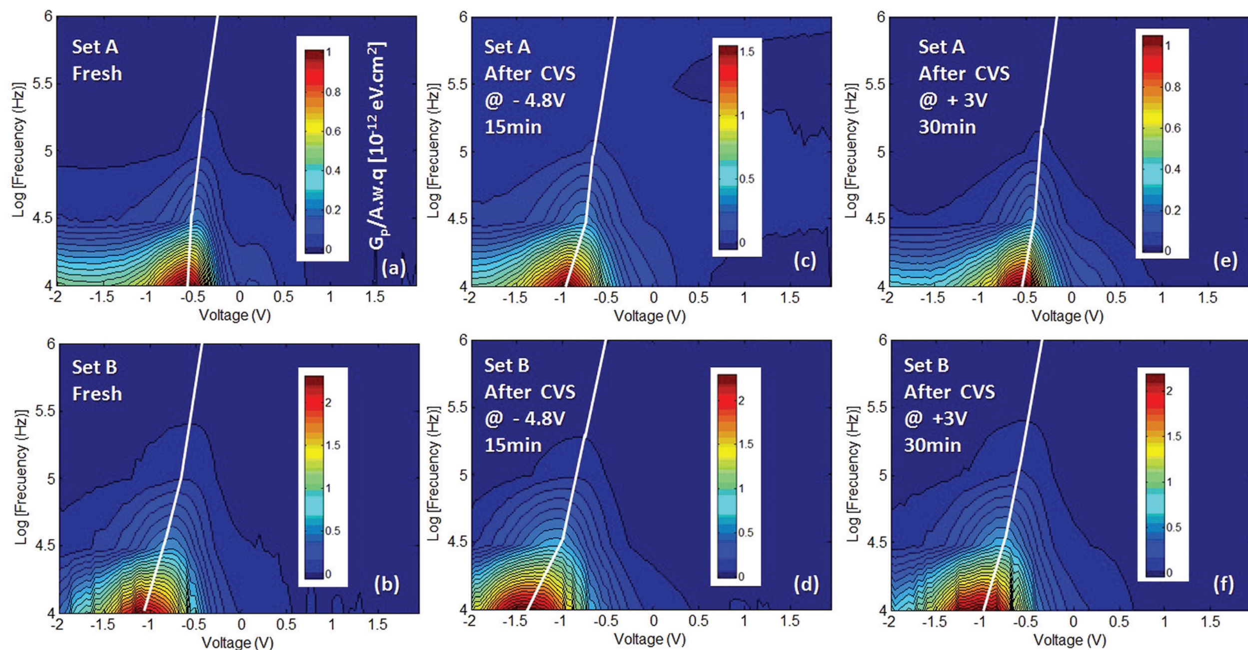

FIG. 8. Maps of the normalized parallel conductance $G_P/A.w.q$, as a function of gate bias V_G and frequency (f) measured at 27 °C. The traces in the middle of conductance plot represent the conductance peaks. (a) and (b) Fresh devices for set A and B, respectively. (c) and (d) after CVS at −4.8 V for 15 min for sets A and B, respectively. (e) and (e) after CVS at +3 V for 30 min for sets A and B, respectively. The traces in the middle of the conductance plots represent the conductance peaks.

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confirmed by XPS in our previous work,[7] by the "weak inversion hump" in the C-V curves (Figure 1), and by the parallel conductance [$G_P/A.w.q$] (Figure 8(a))) generate, under negative stress bias, more positive charge (see Figure 6) and interface states than set B with a higher initial density of interface states. The simultaneous generation of positive charge and interface states suggest that depassivation of the interface is the main mechanism for the generation of positive charge, as stated above.

Moreover, it is important to note the similarity between Figures 8(b) and 8(c), with respect to the frequency shift with gate bias and the magnitude of [$G_P/A.w.q$]. Figure 8(b) correspond to set B with higher density of Ga-O bonds,[7] while Figure 8(c) correspond to set A with an initial lower density of Ga-O bonds,[7] but after CVS at −4.8 V. The similarity suggests that the stress at negative bias depassivates the interface leading to a state as in the case of set B. Therefore, the origin of ΔV_{FB} differences observed in Figure 6 may be attributed to the different densities of passivated Ga-O bonds between the two sets as suggested in Sec. III C.

Figures 8(e) and 8(f) show the parallel conductance [$G_P/A.w.q$] contours after CVS at a positive bias for sets A and B, respectively. Contrary to the previous cases, under this condition, there is not relevant change compared to the fresh case neither in the frequency shift with gate bias, nor the magnitude of [$G_P/A.w.q$]. This observation is a clear indication that the interface does not play a relevant role in degradation under positive bias supporting the interpretation that electron trapping is the main degradation mechanism.

IV. SUMMARY

The results of this paper show that the oxide-semiconductor interface affects differently the degradation under positive and negative bias. The physical reason for such a difference lies in the origin of the generated charge that shifts the V_{FB}. At positive bias, the lack of generation of interface states and the insensitivity to temperature support the assumption that the main degradation mechanism is related to electron trapping in border traps.

For negative bias, two contributions (interface states and bulk traps) dominate depending on the stress conditions: room or high temperature. At room temperature, the positive charge generation is mainly due to the interface contribution, since the accumulation of positive trapped charge is accompanied with generation of interface states. The physical origin of the interface contribution can be understood in terms of the dissociation of the bonds at the interface (i.e., depassivation of the interface). This physical mechanism explains the differences of the V_{FB} between both sets of samples with different density of passivated bonds. At high temperatures, the generation of bulk traps seems to be the dominant contribution supporting the similarity of ΔV_{FB} between both sets of samples.

Further experiments should be performed to confirm this interpretation. The evaluation of the XPS spectra before and after CVS pulses would clarify the correlation of the bonds at the oxide-semiconductor interface with the generation of positive charge and interface states. The overall results show that surface treatment with NH_4OH improves the quality of the interface in term of interface states, but it contributes to the generation of positive charge trapping under negative bias.

ACKNOWLEDGMENTS

The authors gratefully acknowledge I. Krylov (Technion) for providing the samples, and P. Shekhter, S. Fadida (Technion), F. Guarin, G. La Rosa (IBM), B. Kazer, and J. Franco (IMEC) for inspiring discussions. Felix Palumbo is a researcher of CONICET on leave at the Technion. The research leading to these results has received funding from the European Union's—Seventh Framework Programme (FP7/2007-2013) under Grant Agreement No. 299094–MC–CONAT.

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